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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,963	04/23/2001	Sangki Hong	CS99-210	4495

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,963	HONG ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on th cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-12 and 14-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12 and 14-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/04/2003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al. (U.S. 4,536,951) in view of Liu et al. (U.S. 5,693,568).

In reference to claims 1 and 2, Rhodes (Figs.1-5) in a related method to form self-aligned, anti-via interconnects teach providing a semiconductor substrate (4); depositing a metal layer (2, 6, 8) overlying said semiconductor substrate (4), wherein said metal layer comprises aluminum; etching through metal layer (2, 6, 8) to form connective lines; thereafter etching partially through said metal layer (2, 6, 8) to form vias (10); thereafter depositing a dielectric layer (12) overlying said vias, said connective lines (2, 6, 8) and said semiconductor substrate (4); and removing portions of the

dielectric layer (12), thus exposing said vias, therefore, completing said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device (column 2, line 44 – column 4, line 33).

Rhodes et al. fail to teach polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device. However, Liu et al. (Figs.1-9) in a related method to form self-aligned anti-via interconnects teach depositing dielectric layer (51) over a patterned via (40); and polishing down said dielectric layer (50), completing said anti-via interconnect structure (column 7, lines 51 – 55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Rhodes et al. and Liu et al. to enable using polishing processes to finish the anti-via interconnects.

In reference to claim 3, the combined teachings of Rhodes et al. and Liu et al. teach wherein said semiconductor substrate comprises semiconductor devices in and on a silicon substrate covered by an insulating layer (Rhodes et al., column 2, lines 44 – 45, and Liu et al., column 6, lines 39 – 53).

In reference to claim 6, the combined teachings of Rhodes et al. and Liu et al. substantially teach all aspects of the invention but fail to teach wherein the dielectric layer deposited to a thickness of between about 5,000 Angstroms and 20,000 Angstroms. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose,

produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

4. Claims 5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al. ('951) in view of Liu et al. ('568) as applied to claims 1-3 and 6 above, and further in view of Wang et al. (U.S. 6,080,660).

The combined teachings of Rhodes et al. and Liu et al. teach forming an etch-stop layer comprising titanium nitride (Liu et al., column 6, lines 56-62). Rhodes et al. in combination with Liu et al. fail to teach using silicon oxide as a dielectric layer; and depositing an antireflective coating (ARC) layer comprising titanium nitride prior to etch through the metal layer. However, Wang et al. (Figs.2A-2C) in a related method to form interconnect structures teach the steps of performing a partial etch process comprising a timed etch on a metal layer (22); using silicon oxide as a dielectric layer (23); and depositing an antireflective coating (ARC) layer (24) comprising titanium nitride prior to etch through the metal layer (22) (column 3, line 55 – column 4, line 26). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use titanium nitride as an ARC layer and silicon oxide as a dielectric layer

as taught by Wang et al. in the anti-via formation method of Rhodes et al. and Liu et al., since these materials are commonly used in the fabrication of metal interconnects (column 1, lines 34-63).

5. Claims 9-12 and 14-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al. ('951) in view of Liu et al. ('568) and Wang et al. (U.S. 6,080,660).

In reference to claims 9, 10, 14-19, 22 and 23, Rhodes (Figs.1-5) in a related method to form self-aligned, anti-via interconnects teach providing a semiconductor substrate (4); depositing a first metal layer (2) overlying said semiconductor substrate (4), wherein said first metal layer (2) comprises aluminum; depositing an etch stop layer (6) over the first metal layer (2), wherein said etch stop layer (6) comprises titanium; depositing a second metal layer (8) overlying said first metal layer (2), wherein said second metal layer (8) comprises aluminum; etching through said second metal layer (8), and said first metal layer (2) to form connective lines; thereafter etching through said second metal layer (8), stopping at said etch stop layer (6) to form vias (10); thereafter depositing a dielectric layer (12) overlying said vias, said connective lines and said semiconductor substrate (4); and removing portions of the dielectric layer (12), thus exposing said vias, therefore, completing said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device (column 2, line 44 – column 4, line 33).

Rhodes et al. fail to teach polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device. However, Liu et al. (Figs.1-9) in a related method to form self-aligned anti-via

interconnects teach depositing dielectric layer (51) over a patterned via (40); and polishing down said dielectric layer (50), completing said anti-via interconnect structure (column 7, lines 51 – 55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Rhodes et al. and Liu et al. to enable using polishing processes to finish the anti-via interconnects.

Rhodes et al. in combination with Liu et al. fail to teach depositing an antireflective coating (ARC) layer comprising titanium nitride over the second metal layer; and using silicon oxide as a dielectric layer. However, Wang et al. (Figs.2A-2C) in a related method to form interconnect structures teach the steps of depositing an antireflective coating (ARC) layer (24) comprising titanium nitride over a metal layer (22); and using silicon oxide as a dielectric layer (23) (column 3, line 55 – column 4, line 26). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use titanium nitride as an ARC layer and silicon oxide as a dielectric layer as taught by Wang et al. in the anti-via formation method of Rhodes et al. and Liu et al., since these materials are commonly used in the fabrication of metal interconnects (column 1, lines 34-63).

In reference to claims 11, 12, 20 and 21, the combined teachings of Rhodes et al., Liu et al. and Wang et al. teach depositing the first and second metal layers with a thickness of about 10,000 Angstroms (Rhodes et al., column 2, lines 49 – 52). The combination of Rhodes et al., Liu et al. and Wang et al. fail to teach depositing the first metal layer between about 1,000 Angstroms and 10,000 Angstroms and depositing the second metal layer with a thickness of about 3,000 Angstroms to 10,000 Angstroms.

However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dimensional range disclosed by the prior art of record to arrive at the claimed invention.

Conclusion

6. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
7/30/03

George Fourson
Primary Examiner